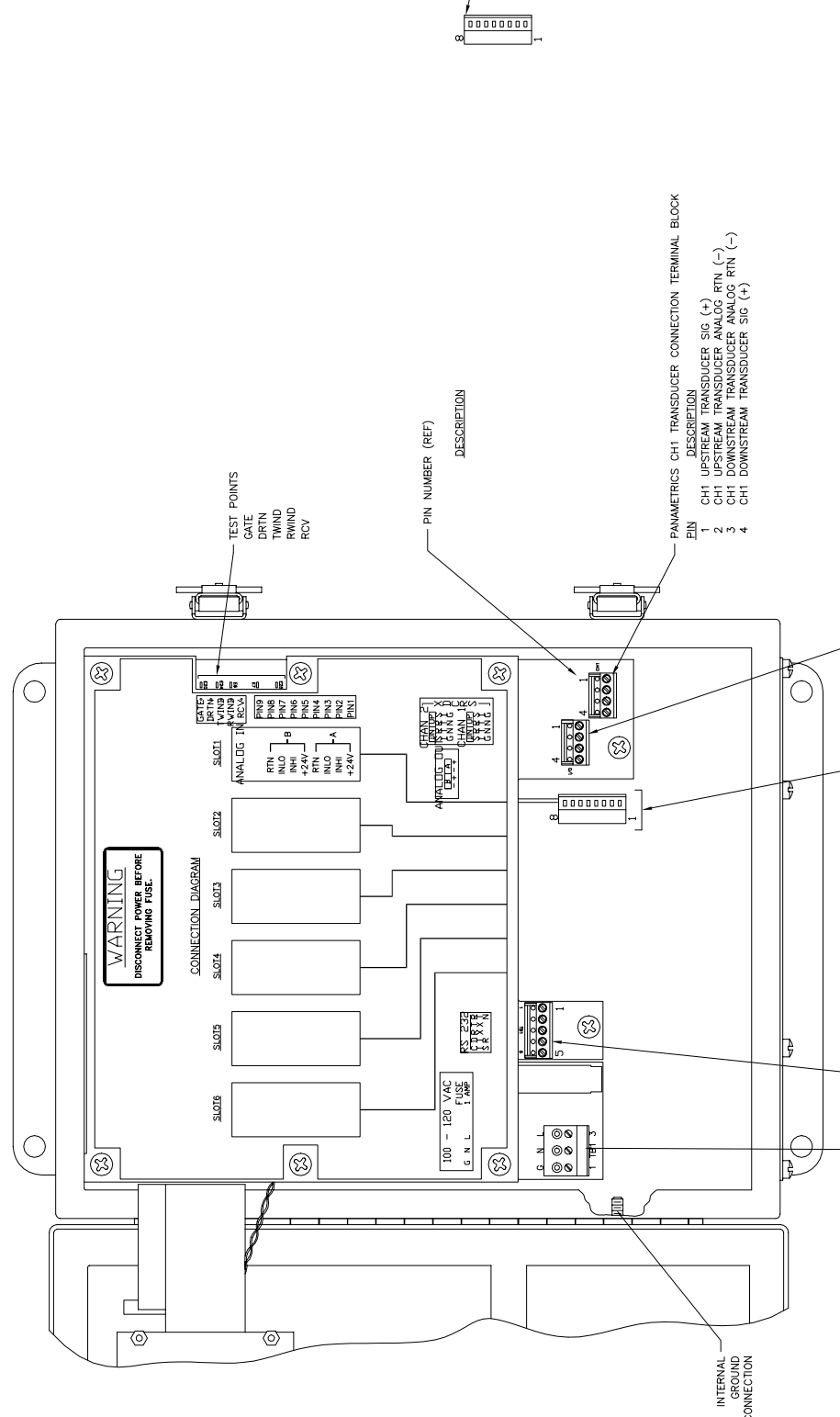


REV	EGD	DATE	DESCRIPTIONS	REV	DATE	DESCRIPTIONS
1		7/29/95	ORIGINATED FOR REV CONTROL	1		REV'D

REV	EGD	DATE	DESCRIPTIONS	REV	DATE	DESCRIPTIONS
1		7/29/95	ORIGINATED FOR REV CONTROL	1		REV'D



DETAIL A - OPTIONS

PIN	DESCRIPTION
8	4-20 mA INPUT B RTN
7	4-20 mA INPUT B INLO
6	4-20 mA INPUT B INHI
5	4-20 mA INPUT B +24V
4	4-20 mA INPUT A RTN
3	4-20 mA INPUT A INLO
2	4-20 mA INPUT A INHI
1	4-20 mA INPUT A +24V

PIN	DESCRIPTION
1	CH1 UPSTREAM TRANSDUCER SIG (+)
2	CH1 UPSTREAM TRANSDUCER ANALOG RTN (-)
3	CH1 DOWNSTREAM TRANSDUCER ANALOG RTN (-)
4	CH1 DOWNSTREAM TRANSDUCER SIG (+)

PIN	DESCRIPTION
1	4-20 mA OUTPUT A SIG
2	4-20 mA OUTPUT A RTN
3	4-20 mA OUTPUT B SIG
4	4-20 mA OUTPUT B RTN

PIN	DESCRIPTION
1	RTN
2	TX
3	RX
4	DTR
5	CTS

REVISIONS	DATE	DESCRIPTIONS
1	7/29/95	ORIGINATED FOR REV CONTROL

DESIGNER	DATE	SCALE	DO NOT SCALE DWG	SHEET 1 OF 1
DRWING NUMBER	702-320	1		
CHECKER				
APPROVED				
ENGINEER				
PROJECT				
TITLE	100-120 VAC WIRING DIAGRAM, GS8688 SINGLE CHANNEL WITH ANALOG INPUTS			
PROJECT NO.	PANAMETRICS WALTHAM, MASS. 02154-3487			